Over-60-GHz Design Technology for an SCFL Dynamic Frequency Divider Using InP-Based HEMT's

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***Abstract*— A toggle operation of 39–63.5 GHz without tuning has been achieved by a digital dynamic frequency divider (DFD). The DFD employs a pair of clocked inverters (CI's) with source-coupled FET logic (SCFL) and uses 0.1-μm–gate InAlAs/InGaAs/InP high electron-mobility transistors (HEMT's) of good uniformity and high performance. On a 2-in wafer, the frequency divider showed a maximum toggle frequency ($f_{\mathrm{tog,max}}$) of 59.1±3.3 GHz and a fabrication yield of 89%. This is the highest operation frequency ever reported for a broad-band digital frequency divider. Comparison of the DFD and the static frequency divider (SFD) showed that the ratio of $f_{\mathrm{tog,max}}$ for the DFD to that for the SFD is much higher than the value expected from the linear-response theory. The comparison also showed that the ratio of the measured $f_{\mathrm{tog\ max}}$ for the DFD to that for the SFD is 1.7, in contrast with the value of two expected from the circuit simulation. Delay-time analysis revealed that this 15% decrease of the ratio is due to the transmission delay of interconnections and charging time for stray capacitance.**

***Index Terms*— Frequency conversion, digital integrated circuits, indium compounds, MODFET integrated circuits.**

I. Introduction

THE InAlAs/InGaAs/InP high electron-mobility transistors (HEMT's) have demonstrated excellent ultrahigh-frequency [1], [2] and low-noise [3] performance and have been used in various monolithic microwave integrated circuits (MMIC's) for the millimeter-wave band, such as low-noise amplifiers [4], [5], high-power amplifiers [6], traveling-wave amplifiers [7], mixers [8], and oscillators [9]. They have also been used in the integration of these kinds of millimeter-wave circuits [10]. Although they have been used in a few digital integrated circuits (IC's) (i.e., 26.7-GHz frequency divider [11]), there have been few such applications because of the difficulty of attaining the larger scale integration which is more common in digital IC's than in MMIC's. Using an electron beam (EB)/photo hybrid T-shaped-gate process and an InP recess-etch stopper in these types of HEMT's and using source-coupled FET logic (SCFL) gates [12], we have been able to make a 40.4-GHz static frequency divider (SFD) [13], 46-Gb/s multiplexer [14], and 40-Gb/s demultiplexer [14] for optical transmission systems. However, for emerging frequency-division applications at frequencies far above 40 GHz, dynamic frequency dividers (DFD's) are the only demonstrated devices. Two types of analog DFD's have recently been reported: a 57–64-GHz regenerative DFD IC using GaAs-based HEMT's [15] and a 75-GHz DFD IC with an injection-locked push–pull oscillator using InP-based HEMT's [16]. These types of DFD's are advantageous in ultrafast operation, but their locking range for a fixed bias condition is intrinsically narrow and they need to be tuned if they are to operate over a broad frequency range [16]. In contrast, digital DFD's not only operate at high speeds, but also have a broad-band operation range without tuning. There have, for example, been reports on a 28–51-GHz DFD IC with dual-ring oscillators gated by transfer gates using GaAs-based HEMT's [17] and on a 25–50-GHz DFD IC with a dynamic toggle flip–flop (DTFF) composed of two clocked inverters (CI's) using GaAs-based heterojunction bipolar transistors (HBT's) [18]. We adopted the latter type of digital DFD's because the basic gate of this type of frequency divider is the same as the one for digital circuits such as the dynamic D flip–flop (D-FF) [19]. This type of frequency divider can, therefore, also be considered a benchmark for the operation frequency of ultrahigh-speed digital IC's in dynamic operation.

In this paper, we describe the design and performance of a digital DFD with a pair of SCFL CI's using InAlAs/InGaAs/InP HEMT's. The advantage of CI's in broad-band operation and the good uniformity and high performance of the HEMT's give this frequency divider 63.5-GHz toggle operation and a 24.5-GHz operation bandwidth without tuning. This frequency divider demonstrates the feasibility of digital circuits operating at more than 60 GHz. In addition, comparison of this DFD with the SFD using a static toggle flip–flop (STFF) composed of a pair of D-latches shows that the DFD operates at a speed higher than that predicted from the delay time when using linear response theory. Moreover, a delay-time analysis for the fabricated DFD and SFD shows that interconnections and stray capacitance decrease the speed of IC's, and also shows how to further increase the operation speed of the DFD.

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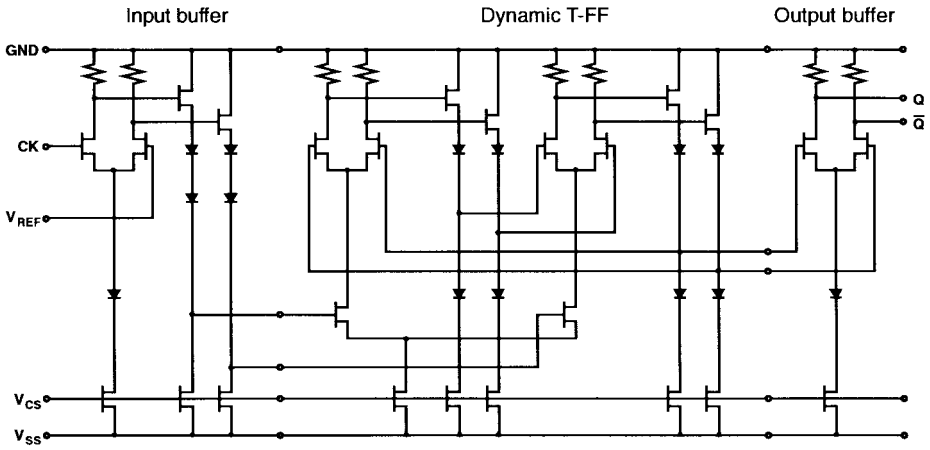

Fig. 1. Circuit diagram of the SCFL DFD using a DTFF composed of two CI's.

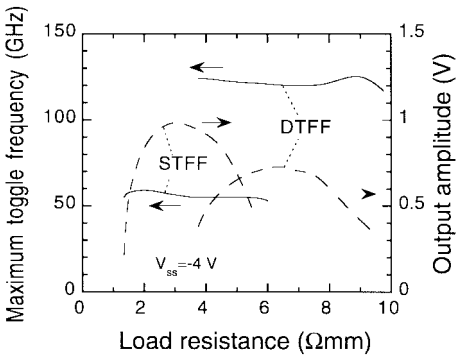

Fig. 2. Calculated dependence of the maximum toggle frequency and the output amplitude of the DTFF and the STFF on the load resistance. The output amplitude is calculated at 120 GHz for the DTFF and 55 GHz for the STFF.

II. Design

As shown in Fig. 1, the SCFL DFD consists of an input buffer converting a single-ended input signal to a differential signal, DTFF composed of two CI's, and an output buffer driving 50-Ω lines. Fig. 2 shows the calculated dependencies (by circuit simulation) of the maximum toggle frequency ($f_{\mathrm{tog\,max}}$) and the output amplitude (V_{out}) on the load resistance (R_L) of the DTFF. The corresponding dependencies are also shown for the STFF using two D-latches [13]. The dependence of $f_{\mathrm{tog\,max}}$ on R_L is weak for both circuits and the ratio of $f_{\mathrm{tog\,max}}$ for the DTFF to that for the STFF is about two. Because of the weak dependence of $f_{\mathrm{tog\,max}}$ on R_L, the design focused on stable operation (i.e., large output amplitude) rather than high-speed operation: the designed R_L values for the DTFF and the STFF were 6.5 and 2.25 $\Omega\cdot$mm, respectively.

The minimum R_L for toggle operation for the DTFF is approximately 3.7 $\Omega\cdot$mm , whereas the corresponding R_L for the STFF is 1.4 $\Omega\cdot$mm. This large minimum R_L for the DTFF is due to the absence of a latching function in the CI. According to linear-response theory as applied to SCFL gates [19], the delay time (τ) for a CI (τ_{CI}) and a D-latch (τ_{DL}) can be approximated as [20]

$$\tau = n\frac{C_{\mathrm{gs}}+C_{\mathrm{gd}}}{g_{m,\,\max}} + R_L C_{\mathrm{gd}}\left(1+n\frac{\langle g_m\rangle}{g_{m,\,\max}}\right) \qquad (1)$$

where C_{gs} is the gate–source capacitance, C_{gd} is the gate–drain capacitance, $g_{m,\max}$ is the maximum transconductance, $\langle g_m\rangle$ is the average transconductance, and n is the number of load transistors for the current switch and source-follower circuit (n is one for the DTFF and two for the STFF). The τ_{CI} can be regarded here as the time constant of discharge for a CI when the CI is initially charged to some signal level. Since the CI does not have a latching function, it has to hold some signal level with a time constant of τ_{CI} in order to transfer the level to the other CI before the level vanishes by discharge. The DTFF, therefore, has some minimum value of R_L for toggle operation, whereas the STFF with a latching function does not have such a limitation. This discharging mechanism is considered to be the reason the DTFF needs a large R_L.

For a short-gate-length HEMT, such as the one used in this paper, the typical values of the C_{gs}, C_{gd}, $g_{m,\max}$, and $\langle g_m\rangle$ are 0.7 pF/mm, 0.3 pF/mm, 1 S/mm, and 0.75 S/mm, respectively. For the R_L used in the design and using (1), the τ_{CI} and τ_{DL} were calculated to be 4.4 and 3.7 ps, respectively. This larger τ_{CI} than τ_{DL} is an example of the larger τ_{CI} due to the larger R_L in a CI than that in a D-latch originated from the level-holding mechanism described above. Using the relation expressed as [19]

$$f_{\mathrm{tog\,max}} = \frac{1}{2\tau} \qquad (2)$$

the ratio of $f_{\mathrm{tog\,max}}$ for the DTFF to that for the STFF is calculated to be 0.8. In contrast, the corresponding ratio obtained by circuit simulation is two (see Fig. 2). The discrepancy between these ratios suggests some speed-up mechanism of the DTFF which is not accounted for by linear-response theory. Possible mechanisms are the waveform-clip effect reported for the STFF [20] and the cross-point shift effect reported for the high-speed latching operation flip–flop (HLO-FF) [19].

In the design of high-speed digital circuits, delays caused by interconnections cannot be neglected. We, therefore, minimized the signal path length in order to reduce the signal transit delay through interconnection lines [21]. Due to the smaller scale of circuit for the CI than for the D-latch, the critical signal-path length for a CI was reduced from 450 μm for a D-latch to 300 μm. The output impedances of each

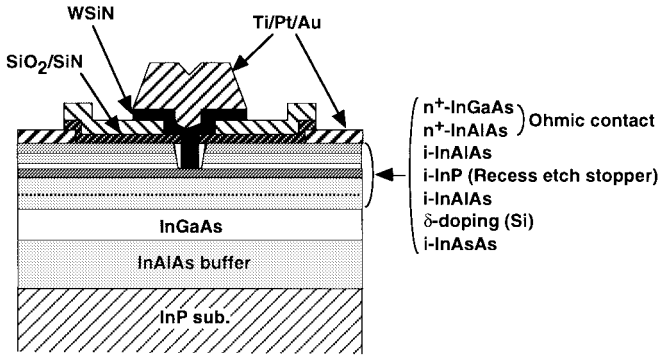

Fig. 3. Structure of an InAlAs/InGaAs/InP HEMT with a T-shaped gate, WSiN refractory gate metal, an SiO_2/SiN bilayer dielectric-film system, and InP recess–etch stopper.

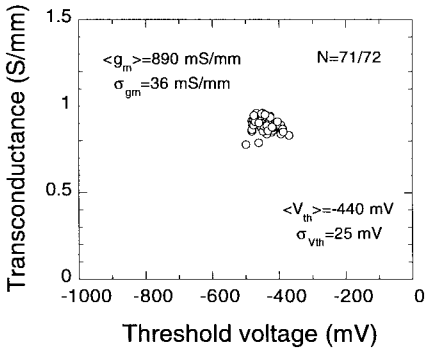

Fig. 4. Transconductance (g_m) versus threshold voltage ($V_{\rm th}$) for 0.1-μm-gate HEMT's on a 2-in wafer.

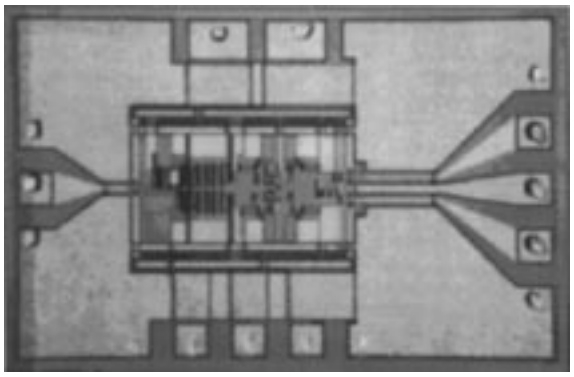

Fig. 5. Photomicrograph of a DFD using 0.1-μm InAlAs/InGaAs/InP HEMT's.

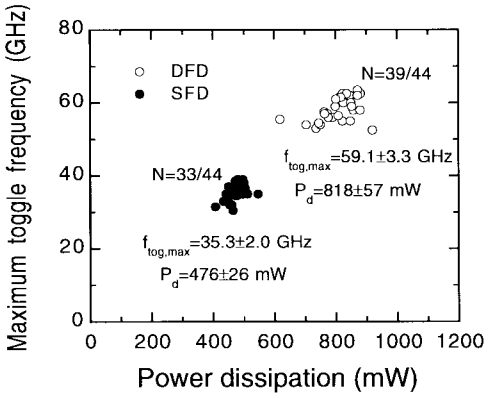

Fig. 6. Distribution of maximum toggle frequency ($f_{\rm tog,\,max}$) and power dissipation (P_d) of the DFD's and SFD's on a 2-in wafer. (DFD: $V_{ss} = -4.6$ V, $V_{cs} = 0.60$ V, $V_{\rm ref} = -2.58$ V. SFD: $V_{ss} = -3.2$ V, $V_{cs} = 0.70$ V, $V_{\rm ref} = -2.20$ V).

stage of the CI's were matched as closely as possible to those of the interconnection lines by optimizing the gatewidth of the FET's [21]. Since the characteristic impedance of interconnection lines is approximately 50 Ω, the optimized gatewidth for the FET's in the DTFF and STFF was 20 μm. The gatewidth for the input buffer was chosen to be 50 μm, so as to give priority to driving capability, whereas that of the output buffer was chosen to be 20 μm, in order to generate sufficient output amplitude and not to reduce the operation speed of the DTFF and STFF.

III. Performance

A. InAlAs/InGaAs/InP HEMT

Fig. 3 shows a cross section of the HEMT, which has a gate length of 0.1 μm. An InAlAs/InGaAs modulation-doped heterostructure lattice-matched to InP substrate was grown by metal–organic chemical vapor deposition (MOCVD). A direct EB writer was used to delineate the footprint of the T-shaped-gate electrode and conventional optical lithography was used to delineate the top part of it [22]. This fabrication process has high accuracy and reproducibility in the size of the gate electrode. WSiN was used as the Schottky-contact metal in order to improve the thermal hardness of the contact [23]. An SiO_2/SiN bilayer dielectric-film system [24] on the semiconductor surface was used to reduce the aspect ratio of the narrow groove for the gate footprint and to completely fill the groove with WSiN. To ensure the uniformity of the gate–recess depth, an InP layer was inserted into the InAlAs barrier layer as a gate–recess–etch stopper [22]. Fig. 4 shows the distribution of threshold voltage ($V_{\rm th}$) and transconductance (g_m) for the HEMT's on a 2-in wafer on which the frequency dividers were fabricated. The use of the InP recess-etch stopper resulted in the standard deviation (σ) of $V_{\rm th}$ being only 25 mV. The g_m of these HEMT's was 890$\pm$36 mS/mm (mean $\pm$ σ). The current–gain cutoff frequency (f_T) of the HEMT's was high and uniform: 164$\pm$7.6 GHz. Seventy-one of the 72 FET's on the wafer worked well.

B. IC Performance

The frequency dividers described in Section II were fabricated using the InAlAs/InGaAs/InP HEMT's described above. Fig. 5 is a photomicrograph of the SCFL DFD, whose chip size is 1.4 $\times$ 0.9 mm. The IC has Schottky diodes for level shifting, metal–insulator–metal (MIM) capacitors with SiN as a dielectric film, and resistors using active layers. The interconnection lines are one-layer metal and air–bridge crossovers which were originally developed for MMIC's. Fig. 6 shows the distribution of $f_{\rm tog,\,max}$ and the power dissipation (P_d) of DFD's and SFD's on the same 2-in wafer. The biases were optimized for high-speed operation. For 44 samples, the fabrication yields of DFD's and SFD's were as high as 89% and 75%. The $f_{\rm tog,\,max}$ values were high and uniform: 59.1$\pm$3.3 GHz for DFD's and 35.3$\pm$2.0 GHz for SFD's, and the respective P_d values were 818$\pm$57 and 476$\pm$26 mW. The

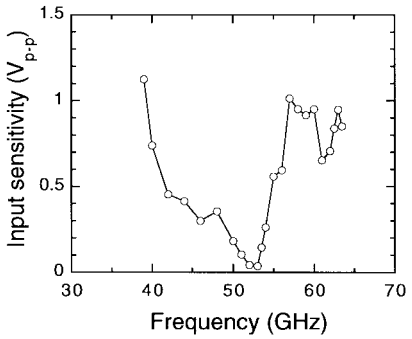

Fig. 7. Input sensitivity versus frequency for a DFD. The frequency of self-oscillation is 52.5 GHz. The ripples are due to residual reflection in the measurement system. ($V_{ss} = -4.6$ V, $V_{cs} = 0.58$ V, $V_{\rm ref} = -2.58$ V, $I_{ss} = 181$ mA, $I_{cs} = 11$ mA, $I_{\rm ref} = 0$ mA).

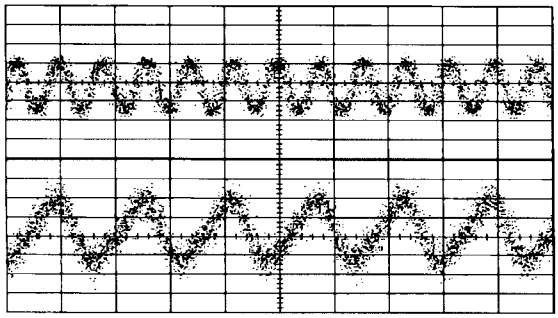

Fig. 8. Input and output waveforms of a DFD. The input (upper) and the output (lower) frequencies are 63.5 and 31.75 GHz, respectively, and their amplitudes are 850 and 140 mV. ($V_{ss} = -4.6$ V, $V_{cs} = 0.58$ V, $V_{\rm ref} = -2.58$ V, $I_{ss} = 181$ mA, $I_{cs} = 11$ mA, $I_{\rm ref} = 0$ mA).

higher P_d of the DFD is due to the lower optimum V_{ss}, which is naturally caused by the lower center level of logic swing ($V_{\rm CL}$) at the output of the current switch, which, in turn, is due to the larger R_L. In fact, the calculated $V_{\rm CL}$ difference of 1.4 V for a typical saturation current of 0.7 A/mm agrees well with the measured optimum V_{ss} difference between the DFD and the SFD. Fig. 7 shows input sensitivity for one of the DFD's, which showed stable toggle operation up to 63.5 GHz. The operation bandwidth, without tuning, is as broad as 24.5 GHz. Fig. 8 shows input and output waveforms of the frequency divider operating at 63.5 GHz. To our knowledge, this operation frequency is the highest ever reported for a digital frequency divider. It is also the highest clock frequency reported for a digital IC synchronized to a clock signal.

C. Delay-Time Analysis

Delay-time analysis was carried out for the CI in the DFD and the D-latch in the SFD (see Fig. 9). The total delay time (τ) for the CI and the D-latch were calculated from the measured average $f_{\rm tog,\,max}$ in Fig. 6 and proven to be 8.5 and 14.2 ps. The intrinsic circuit delay (τ_i) was evaluated from circuit simulations neglecting the parasitic effect caused by interconnection lines and the stray capacitance. The τ_i values calculated for the CI and the D-latch were 4.2 and 8.5 ps, respectively. The signal transit delay (τ_L) through interconnection lines were evaluated (using *LC* line approximation) as $\tau_L = L/v_s$, where the L is the length of an interconnection line and the v_s is the signal-propagation

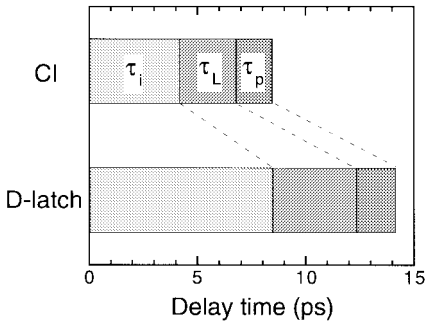

Fig. 9. Delay-time analysis of the CI and the D-latch. τ_i is the intrinsic circuit delay, τ_L is the interconnection-line delay, and τ_p is the parasitic charging delay.

velocity on the line [22]. Note that this *LC* line approximation is valid for interconnection lines used in our design when the frequency is higher than 2 GHz. For the signal–path length, described in Section II, the τ_L values for the CI and the D-latch were calculated to be 2.6 and 3.9 ps, respectively. The τ_p is the remaining delay calculated from the relation $\tau_p = \tau - \tau_i - \tau_L$, which can be interpreted as the charging delay of stray capacitance. This delay was 1.7 ps for the CI and 1.8 ps for the D-latch. Eliminating the latch function and optimizing pattern layouts decreased the τ, τ_i, τ_L, and τ_p values for the CI to be 60%, 49%, 67%, and 94% of the corresponding delays for the D-latch. Consequently, the decrease of the τ is due not only to the decrease of the τ_i, but also to the decrease of the τ_L. However, the decrease of τ_L is smaller than that of τ_i, and the decrease of τ_p is small. Therefore, the τ decrease due to using the CI becomes smaller and the τ for the CI remains 60%, as much as the τ for the D-latch, even though the τ_i decreased to 49%. In addition, the ratios of τ_L and τ_p to τ increase from 27% and 13% to 31% and 20%, respectively. This shows that the reduction of τ_L and τ_p is of more importance in increasing the speed of the DTFF than in increasing the speed of the STFF. The large τ_L is due to the interconnection-line process developed for MMIC's, where the width and space of air–bridges is too large for digital IC's. Accordingly, the optimization of an interconnection–line process is necessary. Decreasing stray capacitance is also necessary because doing so will increase the overall speed of the DTFF.

IV. Conclusion

Digital DFD's employing a DTFF with SCFL CI's and SFD's employing a STFF with SCFL D-latches were fabricated using 0.1-μm InAlAs/InGaAs/InP HEMT's of good uniformity and high performance. They showed excellent yield and uniformity: fabrication yields of 89% and 75% on a 2-in wafer, and $f_{\rm tog,\,max}$ values of 59.1±3.3 and 35.3±2.0 GHz. A DFD achieved a record broad-band toggle operation at 39–63.5 GHz without tuning. Comparison of the DFD and the SFD showed that the ratio of $f_{\rm tog,\,max}$ for the DFD to that for the SFD by circuit simulation is much higher than the expected value using linear-response theory, which shows the existence of some effects that increases the operation speed of the DFD. The comparison also showed that the measured ratio of the $f_{\rm tog,\,max}$ for the DFD to that for the SFD is 1.7, in contrast with the value of two predicted from the circuit simulation.

Delay-time analysis using an *LC* line approximation revealed that this 15% decrease of the ratio is due to the transit delay of interconnections and charging delay for stray capacitance. Reduction of these parasitic delays is, therefore, important for further increasing the operation speed. The fabricated IC showed the highest operation speed of any digital frequency divider and demonstrated that this technology can be used to make digital IC's that can operate at more than 60 Gb/s. The next step to speed-up this type of digital IC is to use fine bilayer interconnection system to shorten the interconnection length. In addition, the use of thick low-permittivity dielectric film like benzocyclobutene (BCB) is effective in decreasing interconnection delay because it increases the propagation speed of a signal. As a result, 80-Gb/s operation of a digital IC will be possible by using these high-speed interconnections.

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